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UFirebird IV - UC7510

Multi-GNSS Single-Frequency Positioning Chip

Foreword

About This Document

This manual provides the schematic diagrams, hardware design considerations, and recommended BOM for the Unicore UC7510 chip.

Target Readers

This manual is intended for technical personnel familiar with GNSS receivers.

Statement

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Revision History

Version	Revision History	Date
R1.0	First release.	Feb. 2026

Document Status

Releases	Status Descriptions	Current Status
Primary	This is a pre-release version with target specifications that are subject to revision.	
Alpha release	This is an alpha release version, which has been preliminarily tested and verified. The content may undergo minor modifications based on user feedback and further testing.	
Production release	The document contains the complete and final specifications.	√

1 Overview

The UC7510 chips include different sub-models, among which UC7510A-00, UC7510A-02, UC7510I-00, and UC7510I-02 are GNSS-only positioning chips, and UC7510A-01 is a GNSS+DR integrated positioning chip.

This document is applicable to all sub-models of the UC7510 chips.

2 Reference Design

The reference circuits for the UC7510 series chips are shown below. When conducting hardware design, please pay attention to the following points:

- V_CORE and V_RF use the same power supply.

- The external TCXO is powered through the LDO_X pin.

- Connect an external RTC crystal.

- Connect an external LNA and SAW filter.

- Use the UART interface for communication.

> **Caution:**
>
> RTC and backup function are the prerequisites of GNSS hot start. If they are not used, the V_BACK pin needs to be connected to ground or V_IO.
>
> It is recommended to design an independent power rail for the antenna to reduce the risk of damage to the chip. If the antenna's power supply and the chip's main power supply use the same power rail, the ESD, surge and overvoltage introduced at the antenna will be directly applied to the main power supply, which may cause damage to the chip.
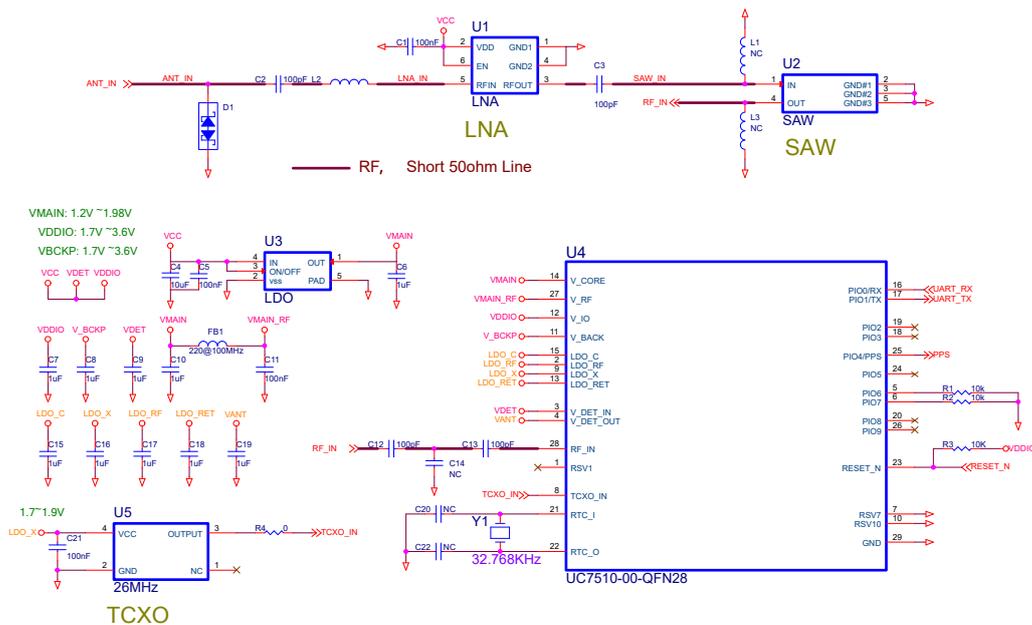

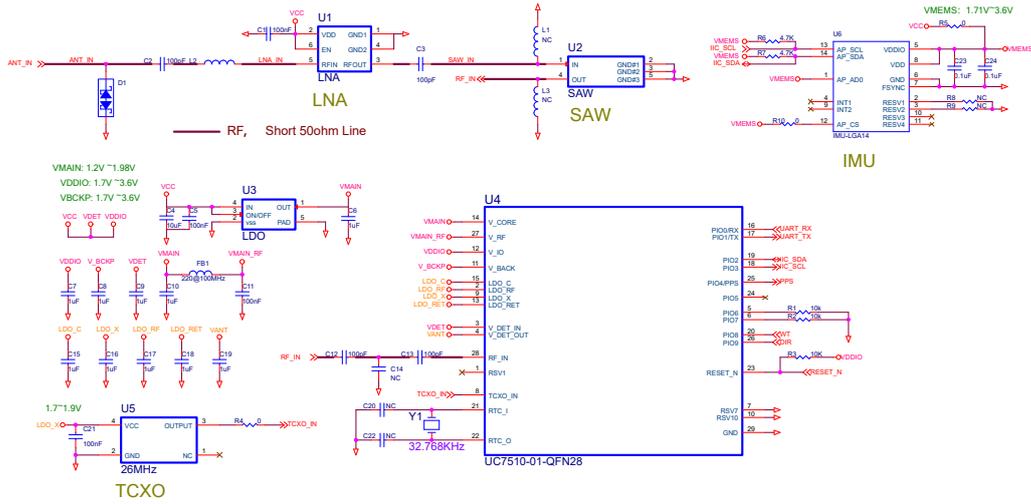Figure 2-1 Schematic Diagram for GNSS Solution

Figure 2-2 Schematic Diagram for GNSS+DR Solution

3 Attention

3.1 Power

For all the power supplies, the ripple voltages must not exceed 50 mV.

In order to avoid the impact of uncontrollable factors and ensure the stability of the chip, it is recommended that the power supply of UC7510 can control the chip's power on and off to restore the system.

V_CORE/V_RF

- V_CORE and V_RF must use the same power supply, and V_RF needs a ferrite bead to filter noise.

- The initial level of V_CORE and V_RF when powered on needs to be less than 0.4 V.

- The power-on ramp of V_CORE and V_RF needs to be monotonic, without plateaus.

- The undershoot and ringing of V_CORE and V_RF when powered on need to be within 5% of the supply voltage.

- Power-on waveform: The time interval from 10% rising to 90% needs to be within 100 μs ~ 10 ms.

- Power-on time interval: The time interval between the power-off (< 0.4 V) to the next power-on needs to be larger than 100 ms.

V_IO

- V_IO needs to be powered no later than V_CORE/V_RF.

- The initial level of V_IO when powered on needs to be less than 0.4 V.

- The power-on ramp of V_IO needs to be monotonic, without plateaus.

- The undershoot and ringing of V_IO when powered on need to be within 5% of the supply voltage.

- Power-on waveform: The time interval from 10% rising to 90% needs to be within 100 μs ~ 10 ms.

- Power-on time interval: The time interval between the power-off (< 0.4 V) to the next power-on needs to be larger than 100 ms.

V_BACK

- The initial level of V_BACK when powered on needs to be less than 0.4 V.

- The power-on ramp of V_BACK needs to be monotonic, without plateaus.

- The undershoot and ringing of V_BACK when powered on need to be within 5% of the supply voltage.

- Power-on waveform: The time interval from 10% rising to 90% needs to be within 100 µs ~ 10 ms.

- Power-on time interval: The time interval between the power-off (< 0.4 V) to the next power-on needs to be larger than 100 ms.

- V_BCKP shall not be floating. When RTC time keeping mode is not used, V_BACK must be connected to ground or V_IO.

3.2 Reset

UC7510 supports system reset. The reset signal is active low and the active time needs to be no less than 1 ms.

3.3 RTC

RTC is usually driven by an on-chip 32768 Hz oscillator, which needs to be connected to an external 32768 Hz crystal. It supports two kinds of connections:

1. Use an external crystal, as shown in the schematic diagrams.

2. Use an external 32768 Hz digital clock signal to directly input to the RTC_I pin, and the RTC_O pin needs to be floating. The clock error is required to be no more than ±0.6Hz/±20ppm.

> **Attention:** When using an external digital clock signal, it is recommended to do ESD protection at the RTC_I pin, and ensure that the signal amplitude must be within 2 V to MIN (V_IO, V_BACK)[1], otherwise the chip may be permanently damaged.

When RTC is not used, connect RTC_I to ground and leave RTC_O floating.

In addition to the general rules of RTC layout and routing, please pay special attentions to the followings:

- Ensure complete GND under the chip and the RTC crystal.

- Place the RTC crystal as close to the chip as possible, and DO NOT place other devices between them.

- Avoid placing any high-power or strong-interference devices, signals, traces, etc. around the RTC crystal.

- It is recommended to implement ground shielding for the RTC circuits.

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[1]The voltages of V_IO and V_BACK must be larger than 2 V.

3.4 TCXO

The TXCO_IN pin is used for connecting an external TCXO of 26 MHz. The TCXO can be powered by LDO_X or an external independent LDO. When V_IO is 1.8 V, use an external independent LDO to power the TCXO.

In order to ensure the chip boots normally, the 26 MHz clock is required to work stably within 10 ms after the chip is powered.

The basic parameters of TCXO are as follows:

- Frequency: 26 MHz ± 0.5 ppm (within all the temperature ranges);

- Short-term frequency stability: < 5 ppb/s.

In addition to the general rules of TCXO layout and routing, please pay special attentions to the followings:

- In order to reduce the impact of heat conduction on the performance of TCXO, it is recommended to maintain the copper void for the layer where the TCXO is placed and its adjacent layers, and keep the reference ground complete for other layers.

- Place the TCXO away from any heat source or interference source, with ground shielding for the surrounding circuits.

- Avoid placing any high-power or strong-interference devices, signals, traces, etc. around the TCXO. Keep a distance of more than 3 times the trace width between the clock trace and other traces.

3.5 Odometer Interfaces

Odometer data can be input to the UC7510A-01 chip via hardware interface or software interface.

> **Note:** The two methods cannot be used at the same time.

3.5.1 Hardware Interface

The PIO8 of the UC7510A-01 chip is used for receiving speed pulse signals from the odometer, and the PIO9 is used for receiving direction signals from the odometer.

The odometer signals of vehicles are generally 12 V and the signal quality is poor. Therefore, signal filtering, optocoupler isolation and level conversion are required before transferring the odometer signals to the UC7510A-01 chip for use.
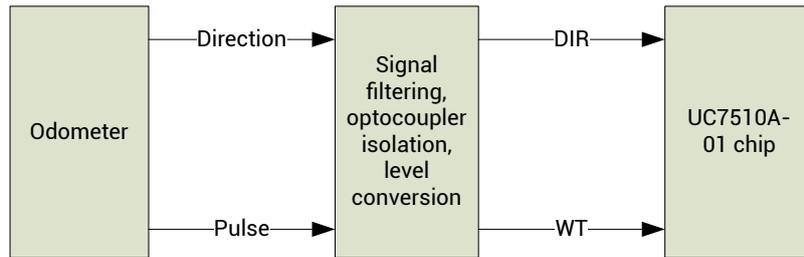

Figure 3-1 Odometer Connection

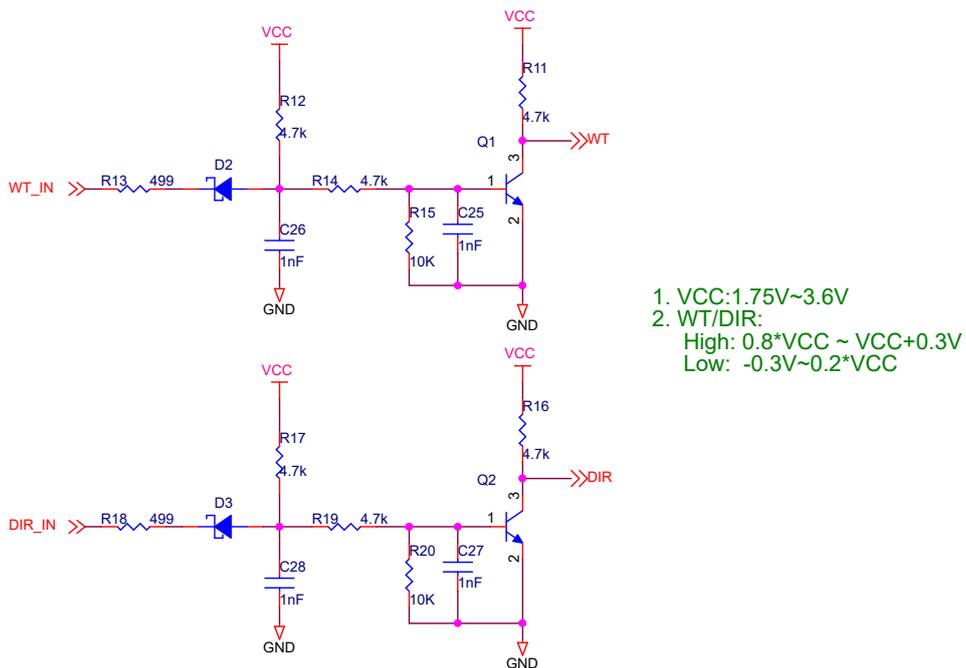## (1) Odometer Reference Circuit and Waveform Diagram

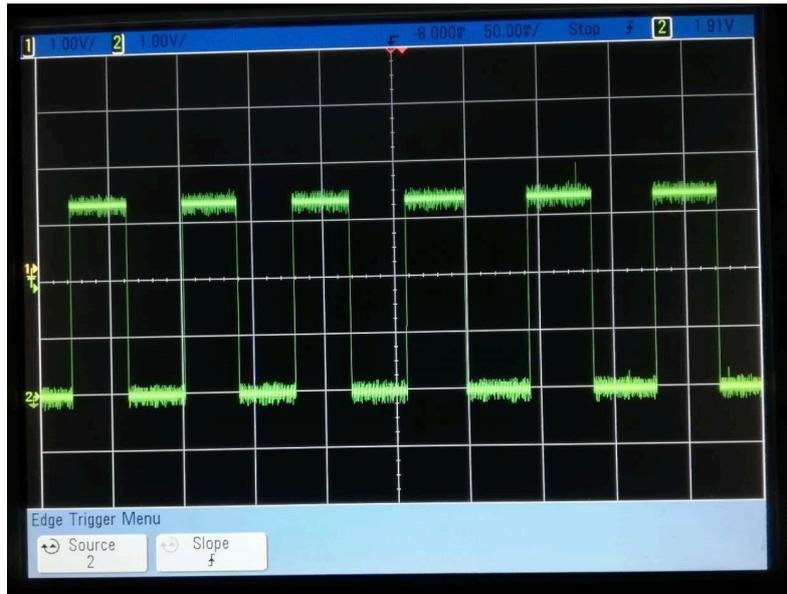Figure 3-2 Odometer Level Conversion Reference Circuit

Figure 3-3 Odometer Waveform Diagram

(2) Odometer Pulse Requirements

1. The odometer pulse is required to be a square wave signal with a frequency not higher than 10 KHz.

2. The distance corresponding to a square wave signal is required to be between 1 cm and 27 cm. For example, if the distance is 20 cm, the output frequency is

    $f = [\,(1000/20) * V/36\,]$ Hz

    where V is the velocity of the vehicle and its unit is km/h.

3. The chip detects the number of rising edges of the square wave signal. Both high-level and low-level durations are required to be no less than 100 μs.

4. If the vehicle is stationary (for example, parking), the voltage level of the WT pin must remain constant.

(3) Odometer Direction Signal

The chip defaults to forward at high level and reverse at low level.

The configuration can be set by commands as shown below. For more information, refer to the *UFirebird IV Protocol Specification*.

* $CFGODOFWD,1
    //forward at high level and reverse at low level

* $CFGODOFWD,0
    //forward at low level and reverse at high level

3.5.2 Software Interface

Speed and direction signals can be input to the UC7510A-01 chip via UART1 using the following command:

Syntax: $ODODATA,time,speed,forward,RSV,RSV,RSV

Example: $ODODATA,091649.00,10000,1,,,

Table 3-1 Parameter Description of ODODATA

Parameter	Format	Description
time	STR	UTC time, in the format of hhmmss.ss hh - Hour mm - Minute ss.ss - Second
speed	UINT	Driving speed; unit: 1e-3 m/s
forward	UINT	Driving direction: 0 - Forward 1 - Reverse
RSV	/	Reserved
RSV	/	Reserved
RSV	/	Reserved

4 Recommended BOM

4.1 Recommended BOM for GNSS Solution

Table 4-1 Recommended BOM for GNSS Solution

Category	Symbol	Description	Model	Manufacturer
10uF capacitor	C4	0402 surface mount capacitor, 10uF ±20% X6S 6.3V	CM05X6S106M06AH	KYOCERA
1uF capacitor	C6 C7 C8 C9 C10 C15 C16 C17 C18 C19	0201 surface mount capacitor, 1uF ±20% X6S 6.3V	CM03X6S105M06AH039	KYOCERA
100nF capacitor	C1 C5 C11 C21	0201 surface mount capacitor, 100nF ±10% X7S 10V	GRM033C71A104KE14D	Murata
100pF capacitor	C2 C3 C12 C13	0201 surface mount capacitor, 100 pF ±10% X7R 25 V	CC0201KRX7R8BB101	YAGEO
TVS	D1	ESD protective diode, DFN0603-2L 1100 W ±18 kV	JEB05UCDS-AH	JIEJIE MICROELECTRONICS CO., Ltd
Ferrite bead	FB1	Ferrite bead, BLM15AG221SN1D	BLM15AG221SN1D	Murata
10 kΩ resistor	R1 R2 R3	0201 surface mount resistor, 10 kΩ, 1/20 W, ±1%	RC0201FR-0710KL	YAGEO
0 kΩ resistor	R4	0201 surface mount resistor, 0Ω <50mΩ 1/	RC0201F	YAGEO

Category	Symbol	Description	Model	Manufacturer
		20W	R-070 RL	
LNA	U1	LNA, Gain=18.5dB, NF=0.6dB, LGA 6-pin	MXDL N16G F	MAXSCEND
SAW	U2	SAW filter, 1582.4MHz, 48.5MHz, 1.4mmx1.1mm	HDF1 588U-B2	HD
LDO	U3	LDO, 300mA, XTDFN-1×1-4L, 1x1x0.4mm	SGM2 036 S-1.8 XXDH 4G/T R	SGMICRO
TCXO	U5	±0.5 ppm, 26 MHz, 2.0mm*1.6mm*0.61mm	X1G0 05371 02001 6	EPSON
Crystal	Y1	32.768 KHz, ±20 ppm, 12.5 pF	X1A0 00171 00011 8	EPSON

4.2 Recommended BOM for GNSS+DR Solution

Table 4-2 Recommended BOM for GNSS+DR Solution

Category	Symbol	Description	Model	Manufacturer
10uF capacitor	C4	0402 surface mount capacitor, 10uF ±20% X6S 6.3V	CM05 X6S1 06M0 6AH	KYOCERA
1uF capacitor	C6 C7 C8 C9 C10 C15 C16 C17 C18 C19	0201 surface mount capacitor, 1uF ±20% X6S 6.3V	CM03 X6S1 05M0 6AH0 39	KYOCERA
100nF	C1 C5	0201 surface mount	GRM0	Murata

Category	Symbol	Description	Model	Manufacturer
capacitor	C11 C21 C23 C24	capacitor, 100nF ±10% X7S 10V	33C7 1A10 4KE1 4D	
100pF capacitor	C2 C3 C12 C13	0201 surface mount capacitor, 100 pF ±10% X7R 25 V	CC02 01KR X7R8 BB10 1	YAGEO
TVS	D1	ESD protective diode, DFN0603-2L 1100 W ±18 kV	JEB0 5UCD S-AH	JIEJIE MICROELECTRONICS CO., Ltd
Ferrite bead	FB1	Ferrite bead, BLM15AG221SN1D	BLM1 5AG2 21SN 1D	Murata
10KΩ resistor	R1 R2 R3	0201 surface mount resistor, 10 kΩ, 1/20 W, ±1%	RC02 01F R-071 0KL	YAGEO
4.7KΩ resistor	R6 R7	0201 surface mount resistor, 4.7 kΩ, 1/20 W, ±1%,	RC02 01F R-074 K7L	YAGEO
0KΩ resistor	R4 R5 R10	0201 surface mount resistor, 0Ω <50mΩ 1/ 20W	RC02 01F R-070 RL	YAGEO
LNA	U1	LNA, Gain=18.5dB, NF=0.6dB, LGA 6-pin	MXDL N16G F	MAXSCEND
SAW	U2	SAW filter, 1582.4MHz, 48.5MHz, 1.4mmx1.1mm	HDF1 588U-B2	HD
LDO	U3	LDO, 300mA, XTDFN-1×1-4L, 1x1x0.4mm	SGM2 036 S-1.8 XXDH 4G/T	SGMICRO

Category	Symbol	Description	Model	Manufacturer
			R	
TCXO	U5	±0.5 ppm, 26 MHz, 2.0mm*1.6mm*0.61mm	X1G005371020016	EPSON
Crystal	Y1	32.768 KHz, ±20 ppm, 12.5 pF	X1A000171000118	EPSON
IMU	U6	6DoF IMU sensor	SMI330	BOSCH

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